Application Serial No. 09/987,

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		)	OFFICIAL.
Björn BENGTSSON		Examiner: A. HE	OFFICIAL
Application Number: 09/987,991		) Group Art Unit: 285	8
Filed: November 16, 2001		) )	RECEIVED
For:	SYSTEM AND METHOD FOR	j	CENTRAL FAX CENTER
	VOLTAGE DIVIDER HAVING A GUARD STRUCTURE	) )	JUL 1 6 2004

## **AMENDMENT**

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In reply to the Office Action dated October 6, 2003, Applicant offers the following amendments and remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this amendment.

Remarks begin on page 11 of this amendment.

Please enter the following amendments to the claims, which are presented in accordance with revised 37 C.F.R. §1.121.

1. (Previously presented) A voltage divider system (102), comprising:
a high voltage impedance element (104), connected to an input node for receiving an input signal;

a low voltage impedance element (106), connected to the high voltage impedance element (104);

at least one guard element (118), the at least one guard element (118) being coupled between the high voltage impedance element (104) and ground;

wherein the at least one guard element (118) comprises at least one capacitive element; and

wherein the at least one guard element (118) further comprises at least one resistive guard element (124) coupled to the at least one capacitive element.

- 2. (Original) The system of claim 1, further comprising a sample node (110) between the high voltage impedance element (104) and the low voltage impedance element (106) for sampling a -reduced voltage representation of the input signal.
- 3. (Original) The system of claim 2, wherein the sample node (110) is connected to a measurement device (116) to perform the sampling.
- 4. (Original) The system of claim 3, wherein the measurement device (116) samples at least one of voltage, current, frequency, and phase.
- (Original) The system of claim 1, wherein the high voltage impedance element
   (104) comprises at least one resistive element.

- 6. (Original) The system of claim 5, wherein the at least one resistive element comprises at least one resistor.
- 7. (Original) The system of claim 6, wherein the at least one resistor comprises a plurality of resistors.
  - 8. (Canceled)
- 9. (Previously presented) The system of claim 1, wherein the at least one capacitive element comprises at least one capacitor.
- 10. (Original) The system of claim 9, wherein the at least one capacitor comprises a plurality of capacitors.
- 11. (Original) The system of claim 1, wherein the at least one guard element (118) comprises at least two guard elements.
- 12. (Original) The system of claim 10, wherein the at least two guard element (118)s comprise three or more guard elements.
  - 13. (Canceled)
- 14. (Previously presented) The system of claim 1, wherein the at least one resistive guard element (124) comprises at least one resistor coupled to the at least one capacitive element.
- 15. (Previously presented) The system of claim 1, wherein the at least one resistive guard element (124) increases a stability of a voltage drop across the high voltage impedance element (104).
- 16. (Original) The system of claim 1, wherein the at least one guard element (118) is coaxially mounted around the high voltage impedance element (104).
- 17. (Original) The system of claim 1, wherein the at least one guard element (118) shunts stray capacitive currents to ground.

- 18. (Original) The system of claim 17, wherein the shunted stray capacitive currents stabilize a frequency response of the voltage divider (102).
  - 19. (Previously presented) A method for processing a signal, comprising:
- a) receiving an input signal via an input node (108) connected to a high voltage impedance element (104);
- b) communicating a reduced voltage representation of the input signal from the high voltage impedance element (104) to a low voltage impedance element (106);
- c) coupling at least one guard element (118) between the high voltage impedance element (104) and ground;

wherein the guard element (118) comprises at least one capacitive element; and wherein the at least one guard element (118) further comprises at least one resistive guard element (124), further comprising a step of d) coupling the at least one resistive guard element (124) to the at least one capacitive element.

- 20. (Previously presented) The method of claim 19, further comprising a step of e) sampling the reduced voltage representation of the input signal at a sample node (110) between the high voltage impedance element (104) and the low voltage impedance element (106).
- 21. (Previously presented) The method of claim 20, further comprising a step of f) connecting a measurement device (116) to the sample node (110) to perform the sampling.
- 22. (Previously presented) The method of claim 21, further comprising of a step g) sampling at least one of voltage, current, frequency, and phase in the measurement device (116).
- 23. (Original) The method of claim 19, wherein the high voltage impedance element (104) comprises at least one resistive element.

- 24. (Original) The method of claim 23, wherein the at least one resistive element comprises at least one resistor.
- 25. (Original) The method of claim 24, wherein the at least one resistor comprises a plurality of resistors.
  - 26. (Canceled)
- 27. (Previously presented) The method of claim 19, wherein the at least one capacitive element comprises at least one capacitor.
- 28. (Original) The method of claim 27, wherein the at least one capacitor comprises a plurality of capacitors.
- 29. (Original) The method of claim 19, wherein the at least one guard element (118) comprises at least two guard elements.
- 30. (Original) The method of claim 29 wherein the at least two guard element (118)s comprise three or more guard elements.
  - 31. (Canceled)
- 32. (Previously presented) The method of claim 19, wherein the at least one resistive guard element (124) comprises at least one resistor coupled to the at least one capacitive element.
- 33. (Previously presented) The method of claim 19, wherein the at least one resistive guard element (124) increases a stability of a voltage drop across the high voltage impedance element (104).
- 34. (Original) The method of claim 19, wherein the at least one guard element (118) is coaxially mounted around the high voltage impedance element (104).
- 35. (Original) The method of claim 19, further comprising a step of h) shunting stray capacitive currents to ground via the at least one guard element (118).

- 36. (Original) The method of claim 35, wherein the shunted stray capacitive currents stabilize a frequency response.
  - 37. (Previously presented) A voltage divider system, comprising:

high voltage impedance means (104), connected to an input node for receiving an input signal;

low voltage impedance means (106), connected to the high voltage impedance means (104);

at least one guard means (118), the at least one guard means (118) being coupled between the high voltage impedance means (104) and ground;

wherein the at least one guard means (118) comprises at least one capacitive element; and wherein the at least one guard means (118) further comprises at least one resistive guard means (124) coupled to the at least one capacitive element.

- 38. (Original) The system of claim 37, further comprising a sample node (110) between the high voltage impedance means (104) and the low voltage impedance means (106) for sampling a -reduced voltage representation of the input signal.
- 39. (Original) The system of claim 38, wherein the sample node (110) is connected to a measurement means (116) to perform the sampling.
- 40. (Original) The system of claim 39, wherein the measurement means (116) samples at least one of voltage, current, frequency, and phase.
- 41. (Original) The system of claim 37, wherein the high voltage impedance means (104) comprises at least one resistive element.
- 42. (Original) The system of claim 41, wherein the at least one resistive element comprises at least one resistor.

- 43. (Original) The system of claim 42, wherein the at least one resistor comprises a plurality of resistors.
  - 44. (Canceled)
- 45. (Previously presented) The system of claim 37, wherein the at least one capacitive element comprises at least one capacitor.
- 46. (Original) The system of claim 45, wherein the at least one capacitor comprises a plurality of capacitors.
- 47. (Original) The system of claim 37, wherein the at least one guard means (118) comprises at least two guard means.
- 48. (Original) The system of claim 47, wherein the at least two guard means comprise three or more guard means.
  - 49. (Canceled)
- 50. (Previously presented) The system of claim 37, wherein the at least one resistive guard means comprises at least one resistor coupled to the at least one capacitive element.
- 51. (Previously presented) The system of claim 37, wherein the at least one resistive guard means (124) increases a stability of a voltage drop across the high voltage impedance element (104).
- 52. (Original) The system of claim 37, wherein the at least one guard means (118) is coaxially mounted around the high voltage impedance means (104).
- 53. (Original) The system of claim 37, wherein the at least one guard means (118) shunts stray capacitive currents to ground.
- 54. (Original) The system of claim 53, wherein the shunted stray capacitive currents stabilize a frequency response of the voltage divider (102).

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55. (Previously presented) A voltage divider (102), comprising:

a plurality of series-connected high voltage resistors (114a, 114b ... 114n), the series-connected high voltage resistors (114a, 114b ... 114n) connected to an input node (110) for receiving an input signal;

at least one low voltage resistive element (106), the at least one low voltage resistive element (106) connected to the series-connected high voltage resistors (114a, 114b ... 114n);

at least one capacitive guard (118), the at least one capacitive guard (118) connected between the series-connected high voltage resistors (114a, 114b ... 114n) and ground; and wherein the at least one capacitive guard (118) further comprises at least one resistive

guard (124) coupled to the at least one capacitive guard (118).

- 56. (Original) The voltage divider of claim 55, wherein the at least one capacitive guard (118) comprises a plurality of capacitors.
- 57. (Onginal) The voltage divider of claim 55, wherein the at least one capacitive guard (118) comprises at least two capacitive guards.
- 58. (Original) The voltage divider of claim 57, wherein the at least two capacitive guards comprise three or more capacitive guards.
  - 59. (Canceled)
- 60. (Previously presented) The voltage divider of claim 55, wherein the at least one resistive guard (124) comprises at least one resistor coupled to the at least one capacitive guard (118).
- 61. (Previously presented) The voltage divider of claim 55, wherein the at least one resistive guard (124) increases a stability of a voltage drop across the series-connected high voltage resistors (114a, 114b ... 114n).

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- 62. (Original) The voltage divider of claim 55, wherein the at least one capacitive guard (118) shunts stray capacitive current to ground.
- 63. (Original) The voltage divider of claim 62, wherein the shunted stray capacitive currents stabilize a frequency response of the voltage divider (102).
- 64. (Previously presented) The system of claim 1, wherein the system is mounted on a plurality of circuit boards assembled to a divider stack;

wherein the circuit boards are spaced apart by a distance;

wherein the edge of said circuit boards are fitted with a field control ring to avoid partial discharges; and

wherein said divider stack is mounted inside a shielded tube and mounted in a bushing to provide a high voltage connection.

65. (Previously presented) The system of claim 37, wherein the system is mounted on a plurality of circuit boards assembled to a divider stack;

wherein the circuit boards are spaced apart by a distance;

wherein the edge of said circuit boards are fitted with a field control ring to avoid partial discharges; and

wherein said divider stack is mounted inside a shielded tube and mounted in a bushing to provide a high voltage connection.

66. (New) The system of claim 1, wherein the system is mounted on a plurality of circuit boards assembled to a divider stack;

wherein the circuit boards are spaced apart by a distance; and

wherein the edge of said circuit boards are fitted with a field control ring to avoid partial discharges.

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67. (New) The system of claim 37, wherein the system is mounted on a plurality of circuit boards assembled to a divider stack;

wherein the circuit boards are spaced apart by a distance; and
wherein the edge of said circuit boards are fitted with a field control ring to avoid partial
discharges.